Electronic Version
Stylesheet Version v1.1.1

[IC DESIGN MODELING ALLOWING DIMENSION-DEPENDENT RULE CHECKING]

Abstract

A method, system and program product to model an IC design to include dimensions such as a local width and spacing of IC shapes in a consistent fashion. In particular, the invention uses a core portion of Voronoi diagrams to partition edges of a shape into intervals and assigns at least one dimension to each interval such as a local width and spacing. Dimension assignment can be made as any desirable definition set for width and spacing, e.g., numerical values or continuous dimension-dependent design rules. Design rule checking for dimension-dependent spacing rules given in any arbitrary functional form of width and spacing is possible. Application of the invention can be made anywhere the width and spacing of VLSI shapes play a role, e.g., relative to a single edge, neighboring edges, neighboring shapes, and/or for edges in more than one layer of the IC design.